REMARKS/ARGUMENTS

Applicants received the Office Action dated September 16, 2003, in which the Examiner: (1) rejected claim 15 as anticipated by Garnett et al. (US Patent No. 6,141,718); (2) rejected claims 16-24 as anticipated by Funaya et al. (US Patent No. 6,263,393); and (3) rejected claims 1-8 and 10-14 as obvious over Garnett in view of Funaya. In this Response, claims 1-8 and 10-24 are pending. No claims have been amended. Based on the arguments contained herein, Applicants respectfully request reconsideration and allowance of the pending claims.

Rejections under 35 USC § 102

The standard for a rejection under 35 USC § 102 is anticipation. "To anticipate a claim, the reference must teach every element of the claim." MPEP 2131. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Claim 15, in part, requires, "a plurality of local busses each for transferring data between a processing device and an associated memory module." Applicants submit that Garnett does not teach this limitation. As noted by the Examiner, Garnett teaches a plurality of busses (fig. 2, 22, 24, 26) that transfer data between a processing device (Fig. 2, 14, 16) and a DMA engine 133 (shown in Fig. 17). However, the DMA engine 133 is not a memory module as required in claim 15. Specifically, Garnett teaches that the DMA engine 133 "provides a state machine" that "emulates a device bus DMA operation", "disables a comparator", and "enables gates 115A and 115B connected to the paths 94 and 96" (see col. 15, lines 7-29). Applicants cannot find a teaching or suggestion in Garnett that the DMA engine 133 is a memory module as suggested by the Examiner. Furthermore, Applicants cannot find any teaching in Garnett to suggest "a

plurality of local busses each for transferring data between a processing device and an associated memory module" as required in claim 15.

Furthermore, claim 15 requires "the local busses each include two unidirectional bit lines for each data bit and the cross-bus includes two unidirectional bit lines for each data bit." Garnett does not teach or suggest two unidirectional bit lines line for each data bit of each bus and each cross-bus. Specifically, Garnett shows that busses 22, 24, 26, 92, 94, 96 are bi-directional (see Fig. 6). There is no teaching or suggestion in Garnett that any bus (22, 24, 26, 92, 94, 96) includes two unidirectional bit lines for each data bit. In contrast, claim 15 requires two unidirectional bit lines for each bus and crossbus (see Figure 8, wherein the bi-directional channel bridge 506 includes two separate unidirectional bit lines for bus and cross-bus).

Additionally, claim 15 requires "the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules." Garnett does not teach this limitation. Specifically, as noted by the Examiner, Garnett teaches that the master arbiters 180 allocate access to the bus on a first-come-first-serve basis (see col. 16, lines 37-40). Applicants submit that a first-come-first-serve basis is not the same as providing highest priority for accesses from processing devices to the associated memory modules as required in claim 15. For at least these reasons, separately or in combination, Applicants submit that claim 15 is allowable.

Claim 16, in part, requires "a plurality of busses each for transferring data between a processing device and an associated memory module." Fuyana does not this limitation. Specifically, Fuyana teaches a number of bus bridges 1 coupled to a switch module 2 and a scheduler 3. Further, Fuyana teaches that a host-side bus bridge may receive an interrupt signal and inform an interrupt controller of a host processor. Fuyana also teaches that buffer memories (Fig. 4, 114, 115, col. 12, lines 1-19) may be used in each bus bridge. However, Fuyana does not teach a processing device and an associated memory module as required in claim 16. For at least this reason, Applicants submit that claim 16 all claims that depend from claim 16 are allowable.

Additionally, claim 16 requires, "the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules."

Fuyana teaches that data can be stored into cells in order to increase speed of the switch module 2 (see col. 4, lines 47-col. 5, lines 48). However, Fuyana does not teach providing highest priority for accesses from processing device to the associated memory modules as required in claim 16. For at least these reasons, separately or in combination, Applicants submit that claim 16 and all claims that depend from claim 16 are allowable.

Rejections Under 35 USC § 103

To reject a claim under 35 USC § 103, the examiner must establish prima facie obviousness. One factor required to establish prima facie obviousness of a claimed invention is that all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981 (CCPA 1974). See MPEP 2143.03. Applicant traverses the §103 rejections and respectfully submits that the examiner has not established a prima facie case of obviousness because the cited art does not teach or suggest all the claim limitations.

Claim 1 requires "a plurality of busses each configured to couple a processing device to a corresponding memory module." As previously explained, neither Garnett nor Funaya teaches or suggests this limitation. Therefore, a combination of Garnett and Fuyana would also be lacking this limitation.

Furthermore, claim 1 requires "the plurality of busses includes two unidirectional bit lines for each data bit and the at least one cross-bus includes two unidirectional bit lines for each data bit, and wherein the bus bridges include a multiplexer for each outgoing bit line that selects from three other incoming bit lines." Neither Garnett nor Fuyana teaches or suggest two unidirectional bit lines line for each data bit of each bus and each cross-bus. Specifically, Garnett shows that busses 22, 24, 26, 92, 94, 96 are single bi-directional busses (see Fig. 6). There is no teaching or suggestion in Garnett that any bus (22, 24, 26, 92, 94, 96) includes two unidirectional bit lines for each data bit. Likewise, Fuyana does not teach or suggest any busses that include two unidirectional bit lines for each data bit. For at least these reasons, Applicants submit that claim 1 and all claims that depend from claim 1 are allowable.

Claim 11 requires "a memory manager providing control signals to bus bridges that couple local busses between a memory module and a processing device to a cross-bus between

the local busses" and "wherein the local busses each include two unidirectional bit lines for each data bit and the cross-bus includes two unidirectional bit lines for each data bit." As previously explained, neither Garnett nor Fuyana teaches or suggests local busses between a memory and a processing device. Additionally, as previously explained, neither Garnett nor Fuyana teaches or suggests local busses that each include two unidirectional bit lines for each data bit. Additionally, neither Garnett nor Fuyana teaches or suggests a cross-bus includes two unidirectional bit lines for each data bit. For at least these reasons, Applicants submit that claim 11 and all claims that depend from claim 11 are allowable.

Conclusion

In the course of the foregoing discussions, applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art which have yet to be raised, but which may be raised in the future.

Applicant submits that this response constitutes a complete response to all of the issues raised in the office action of January 8, 2003. Applicant has responded to the various rejections under 35 USC §102(b) and §103. In view of the foregoing amendments and remarks, applicant submits that all pending claims are now in condition for allowance, and an early notice to that effect is earnestly solicited. The examiner is invited to contact the undersigned if a telephone interview might prove helpful in resolving this application.

If any fees are inadvertently omitted or if any additional fees are required or have been overpaid, please appropriately charge or credit those fees to LSI Logic Corporation Deposit Account Number 12-2252/5201-20400/DJK.

Respectfully submitted,

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